



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. RA001C10)

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AUG 28 2000

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Entered

In the Application of:)
FARMWALD ET AL.)
Serial No: 09/514,872)
Filed: FEBRUARY 28, 2000)
Title: METHOD AND APPARATUS FOR)
CONTROLLING A SYNCHRONOUS)
MEMORY DEVICE)

Group
Art Unit: 2781

Before
Examiner: G. Auve'

Assistant Commissioner for Patents
Washington, DC 20231

AMENDMENT

Dear Sir:

In response to the Office Action, mailed August 1, 2000, kindly amend the application as follows:

IN THE CLAIMS:

1 16. (Amended) A memory controller for controlling a synchronous
2 memory device, the memory controller comprising:
3 output driver circuitry to output data wherein:
4 the output driver circuitry outputs a first portion of
5 data in response to a rising edge transition of a first
6 external clock signal; and
7 the output driver circuitry outputs a second portion of
8 data in response to a falling edge transition of the first
9 external clock signal; and